Semester	V	Course Title	HDL Lab	Course Code	18 ECL 58
Teaching Period	50 Hours	L – T – P – TL*	0 – 0 – 3 – 3	Credits	2
CIE*	40 Marks	SEE*	60 Marks	Total	100 Marks

CREDITS- 02

Course Objectives:

- Understand the concepts of CAD tool to write HDL programs.
- Realize the program to simulate and synthesize the digital design.
- Select Verilog or VHDL for a given Abstraction level and program FPGAs/CPLDs to synthesize the digital designs.
- Interface the external hardware to FPGAs/CPLDs through I/O ports.

Note: Programming can be done using any compiler. Download the programs on a FPGA / CPLD board and performance testing may be done using 32 channel pattern generator and logic analyzer apart from verification by simulation with tools such as Altera/Modelsim or equivalent.

Laboratory Experiments

PART - A PROGRAMMING

1. Write Verilog code to realize all the logic gates

2. Write the verilog program for the following combinational design with test bench to verify it:

a. 2 to 4 decoder realization using NAND gates in structural description.

b. 8 to 3 encoder with priority and without priority using behavioural model.

c. 8 to 1 multiplexer using case statement and if statements.

d. 4 bit binary to gray converter using 1-bit gray to binary converter, 1-bit adder and subtractor.

e. Multiplexer and Demultiplexer using case statement.

f. 4 bit comparator.

e. 4 bit parity generator.

3. Write a VHDL and Verilog code to describe the functions of a Half Adder, Half Subtractor, Full Adder and Full Subtractor using three modeling styles. Write test bench with appropriate input patterns to verify the modeled behaviour.

4. Write a Verilog code to model 32- bit ALU using the schematic diagram shown below

• ALU should use combinational logic to calculate an output based on the four bit op-code input.

• ALU should pass the result to the out bus when enable line in high, and tri-state the out bus when the enable line is low.

• ALU should decode the 4 bit op-code according to the example given below.

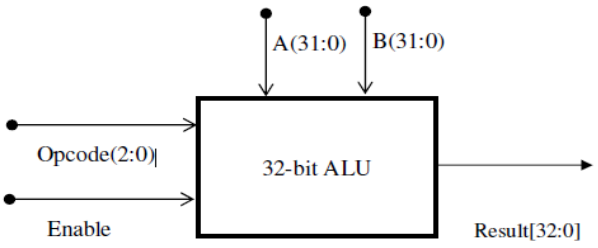

Figure 1 ALU top level block diagram

Opcode(2:0)	ALU Operation	Remarks	
000	A + B	Addition of two numbers	Both A and B are in two's complement format
001	A – B	Subtraction of two numbers	
010	A + 1	Increment Accumulator by 1	A is in two's complement format
011	A - 1	Decrement accumulator by 1	
100	A	True	Inputs can be in any format
101	A Complement	Complement	
110	A OR B	Logical OR	
111	A AND B	Logical AND	

Table 1 ALU Functions

5. Write Verilog code for SR, D and JK and verify the flip flop.

6. Design a 4-bit BCD (Synchronous and Asynchronous reset) Up/Down Counter with Loadable Count.

PART - B

INTERFACING

1. Write HDL code to display messages on 16x2 LCD display.
2. Write HDL code to interface Hex key pad and display the key code on 7-segment LED display.
3. Write HDL code to control speed, direction of DC motor and Stepper motor.
4. Write HDL code to accept Analog input signal from temperature sensor and display the digital output data on LCD or 7-segment LED display.
5. Write HDL code to generate - Sine, Square, Triangle and Ramp waveforms using DAC with different frequency.
6. Write HDL code using FSM to simulate Elevator operation with 4x4 hex key pad input and display the output in LCD.
7. Write HDL code to implement ADC & DAC interface with FPGA.
8. Write HDL code to implement a serial communication interface with FPGA.

Course outcomes:

- Understand the design of combinational logic circuits and write the verilog program, test bench and simulate it.
- Realize the sequential logic circuits in behavioural level abstractions and write the verilog program, test bench and simulate it.
- Synthesize Combinational and Sequential logic circuits on FPGAs/CPLDs and test the hardware.
- Interface the external hardware to the FPGAs/CPLDs and obtain the desired output.